REMARKS

Favorable reconsideration of this application is requested in view of the following remarks.

Claim 1 has been amended to remove a phrase "so that a shape of the cavity is altered to coincide with outer dimensions of the mounted electronic component". Claim 1 is further amended to include limitations of original claim 5 in addition to editorial revisions and clarify that at least two cavities are formed in the first electrical insulating sheet and that the first cavity is covered by the second electrical insulating sheet and the second cavity is connected with the third cavity formed in the second electrical insulating sheet so that a height of each cavity corresponds to a height of a respective electronic component to be mounted in the cavity as supported by Figs. 17, 18A-B, and 19B and the original specification at page 7, lines 10-13, and page 27, line 29 – page 28, line 18; accordingly, claim 5 has been canceled.

Claims 25 and 26 have been added as supported by the original specification at page 7, lines 10-13.

Claim 1 has been rejected under 35 U.S.C. 112, first paragraph, as not complying with the written description requirement. Applicants respectfully traverse this rejection.

Claim 1 does not require that "so that ... outer dimensions of the mounted electronic component". Accordingly, this rejection is moot and should be withdrawn. Applicants do not concede the correctness of this rejection.

Claims 1-5 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kanzawa et al (U.S. Patent Application Publication No. 2004/0078969) in view of Kwong (U.S. Patent No. 6732428). Applicants respectfully traverse this rejection.

Kanzawa discloses neither a method of manufacturing a component built-in-module that includes more than one electronic components, steps of providing cavities

with different heights corresponding to those of the respective electronic components having different heights to be mounted in the cavities by laminating the second electrical insulating layer having a cavity on the first electrical insulating layer, steps of forming the via hole penetrating through the third electrical insulating sheet and filling the via hole with a conductive resin paste, which must be carried out after the third electrical insulating sheet is produced, or a step of stacking the first wiring board on which the first and the second electronic components are placed, the third electrical insulating sheet in which the cavities have been formed, and the second wiring board so that the first electronic component is built in the first cavity and the second electronic component is build in the second cavity combined with the third cavity, in addition to a step of producing cavities throughout the first electrical insulating sheet as claim 1 requires. Instead, Kanzawa discloses a method of manufacturing a component built-in-module that includes one electronic component and steps of placing the component on projecting electrodes, injecting resin into the gap between the component and the carrier, and superposing an electrical insulating layer in which the through holes have been formed and filled with a via paste on the carrier on which the projecting electrodes and the electronic component are placed (see Figs. 10-13, para. [0073] at page 3 and paras. [0080] - [0082] at page 4). In Kanzawa, the cavity and the through holes are formed on the separate carriers, and the electronic component is placed in the cavity before the projection (see Figs. 11 and 12). Accordingly, claim 1 is distinguished from Kanzawa.

Even if Kwong discloses a method of manufacturing a component built-in-module that includes more than one electronic components and cavities whose sizes correspond to those of the respective electronic components to be mounted therein, Kwong does not disclose how the cavities are formed to accommodate the sizes of respective electronic components to be mounted in the cavities (see Figs. 1 and 2 and coln. 2, lines 8-16, coln. 5, lines 31-36, coln. 6, lines 16-25, and coln. 9, lines 43-49). In addition, Kwong does not disclose how to position an electronic component in the respective cavity. Moreover, Kwong discloses that the electronic components are electrically connected to electrically conductive signal layers through electrically conductive pads (see Fig. 2 and coln. 7, lines 23-26 and coln. 8, lines 4-19) and does not disclose the steps of forming a via hole and

filling the via hole. Thus, Kwong fails to disclose a step of stacking the first wiring board on which the first and the second electronic elements are placed, the third electrical insulating sheet, and the second wiring board so that the via hole is disposed between the first wiring pattern and the second wiring pattern.

Therefore, even if Kwong were combined with Kanzawa so that sizes of cavities of Kanzawa correspond to the sizes of the respective electronic components to be mounted in the cavities, Kwong does not remedy the deficiencies of Kanzawa regarding the steps of forming the via hole thorough the third electrical insulating layer, filling the hole with a conductive resin paste, and stacking the first wiring board on which the first and the second electronic elements are placed, the third electrical insulating sheet in which the cavities have been formed, and the second wiring board. Accordingly, claim 1 is distinguished from Kanzawa in view of Kwong, and this rejection should be withdrawn.

In view of the above, Applicants request reconsideration of the application in the form of a Notice of Allowance.

Respectfully submitted,

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